Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1 – 54. (Canceled)

55. (currently amended) A chip package, ~~circuit component, used to be connected to a substrate comprising a first pad with a sidewall not covered by a solder mask,~~ comprising:

a semiconductor device;

a substrate comprising a first pad with a sidewall not covered by a solder mask,

a metal pillar between ~~over~~ said semiconductor device and said substrate, wherein said metal pillar has a thickness of between 10 and 100 microns;

a metal layer between ~~over~~ said metal pillar and said substrate, wherein said metal layer has a bottom surface having a first region ~~partially~~ covered by said metal pillar and a second region ~~partially~~ not covered by said metal pillar; and

a solder metal between ~~over~~ said metal layer and said substrate, wherein said solder metal is ~~used to be~~ bonded to said first pad.

56. (canceled)

57. (currently amended) The chip package ~~circuit component~~ of Claim 55, wherein the distance between a sidewall of said metal layer and a sidewall of said metal pillar is greater than 0.2 microns.

58. (currently amended) The chip package ~~circuit component~~ of Claim 55, wherein said semiconductor device comprises a second pad and a passivation layer, said second pad exposed by an opening in said passivation layer, wherein said metal pillar is between ~~over~~ said second pad and said substrate.

59. (currently amended) The chip package ~~circuit component~~ of Claim 58 further comprising a barrier layer between said metal pillar and said second pad.

60. (new) The chip package of Claim 55, wherein said substrate comprises a ball grid array substrate.

61. (new) The chip package of Claim 55 further comprising a contact ball under said substrate, wherein said semiconductor device is over said substrate.

62. (new) The chip package of Claim 55 further comprising an underfill between said semiconductor device and said substrate.

63. (new) The chip package of Claim 55 further comprising a molding compound between said semiconductor device and said substrate.

64. (new) The chip package of Claim 55, wherein said substrate further comprises a second pad neighboring to said first pad and having an edge not covered by a solder mask, and wherein no solder mask traverses between said first and second pads

65. (new) The chip package of Claim 55, wherein said first region is substantially coplanar with said second region.